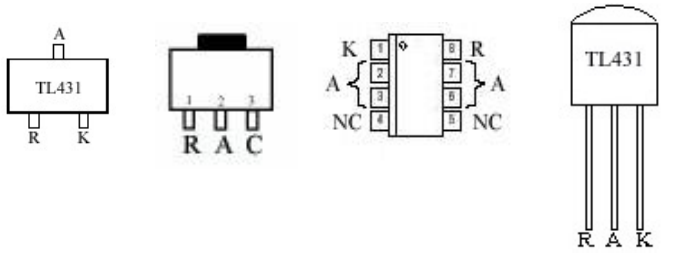
TL431

FEATURES

- Programmable Output Voltage to 40V
- Low Dynamic Output Impedance 0.2Ω
- Sink Current Capability of 0.1 mA to 100 mA
- Equivalent Full-Range Temperature Coefficient of 50 ppm/°C
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage
- Fast Turn on Respons
- TO-92, SOP- 8, SOT-89 or SOT-23 packages

PIN CONNECTIONS

Top View

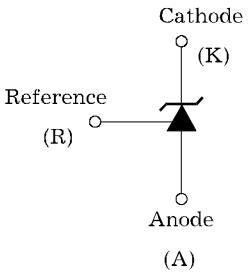


SOT-23 SOT-89 SOP-8 TO-92

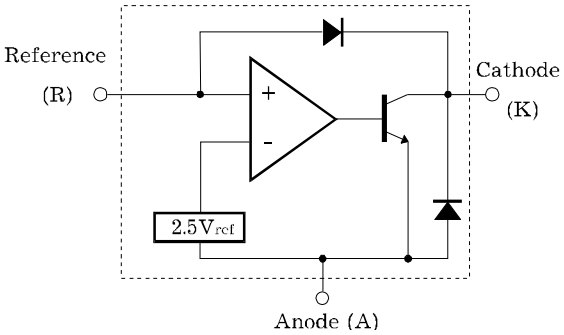
DESCRIPTION

The TL431A is a three-terminal adjustable regulator series with a guaranteed thermal stability over applicable temperature ranges. The output voltage may be set to any value between Vref (approximately 2.5 volts) and 40 volts with two external resistors. These devices have a typical dynamic output impedance of 0.2Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacement for zener diodes in many applications.
The TL431A is characterized for operation from -0°C to +85°C.

SYMBOL



FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operating temperature range applies unless otherwise specified)

Characteristic	Symbol	Value	Unit
Cathode Voltage	V_{KA}	40	V
Cathode Current Range (Continuous)	I_K	-100 ~ 150	mA
Reference Input Current Range	I_{REF}	-0.05 ~ +10	mA
Power Dissipation at 25°C: TO – 92 Package ($R_{\theta JA}$ = 178°C/W) SOT – 23 Package ($R_{\theta JA}$ = 625°C/W)	P_D	 0.7 0.2	 W W
Junction Temperature Range	T_J	0 ~ 150	°C
Operating Temperature Range	T_g	0 ~ 70	°C
Storage Temperature Range	T_{stg}	-65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Cathode Voltage	V_{KA}		V_{REF}		40	V
Cathode Current	I_K		0.5		100	mA

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, $V_{KA} = V_{REF}$, I_K = 10mA unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Input Voltage	V_{REF}	$V_{KA} = V_{REF}$, I_K = 10mA	2.475	2.495	2.505	V
Deviation of Reference Input Voltage Over Full Temperature Range	$V_{REF(dev)}$	$T_{min} \le Ta \le T_{max}$		3	17	mV
Ratio of Change in Reference Input Voltage to the Change in Cathode Voltage	$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	ΔV_{KA} = 10V-V_{REF} ΔV_{KA} = 36V- 10V		-1.4 -1.0	-2.7 -2.0	mV/V
Reference Input Current	I_{REF}	R_1 = 10KΩ, R_2 = ∞		1.8	4	μA
Deviation of Reference Input Current Over Full Temperature Range	$I_{REF(dev)}$	R_1 = 10KΩ, R_2 = ∞		0.4	1.2	μA
Minimum Cathode Current for Regulation	$I_{K(min)}$			0.25	0.5	mA
Off-State Cathode Current	$I_{K(off)}$	V_{KA} = 40 V, V_{REF} = 0		0.26	0.9	μA
Dynamic Impedance	Z_{KA}	I_K = 1mA to 100 mA , f ≤ 1.0KHz		0.22	0.5	Ω

TEST CIRCUITS

Fig.1. Test Circuit for $V_{KA} = V_{REF}$

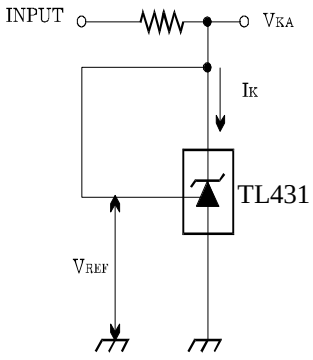
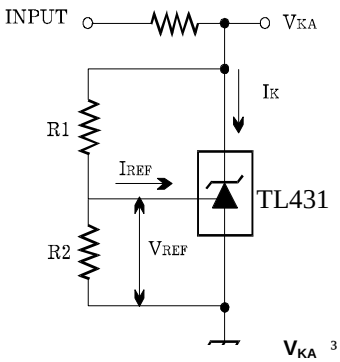
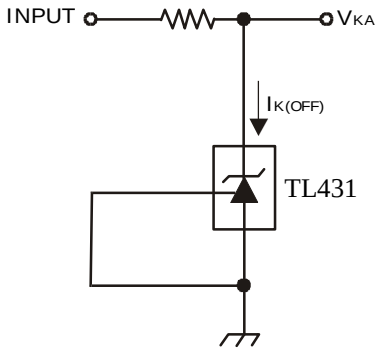


Fig.2. Test Circuit for V_{KA} ³ V_{REF}

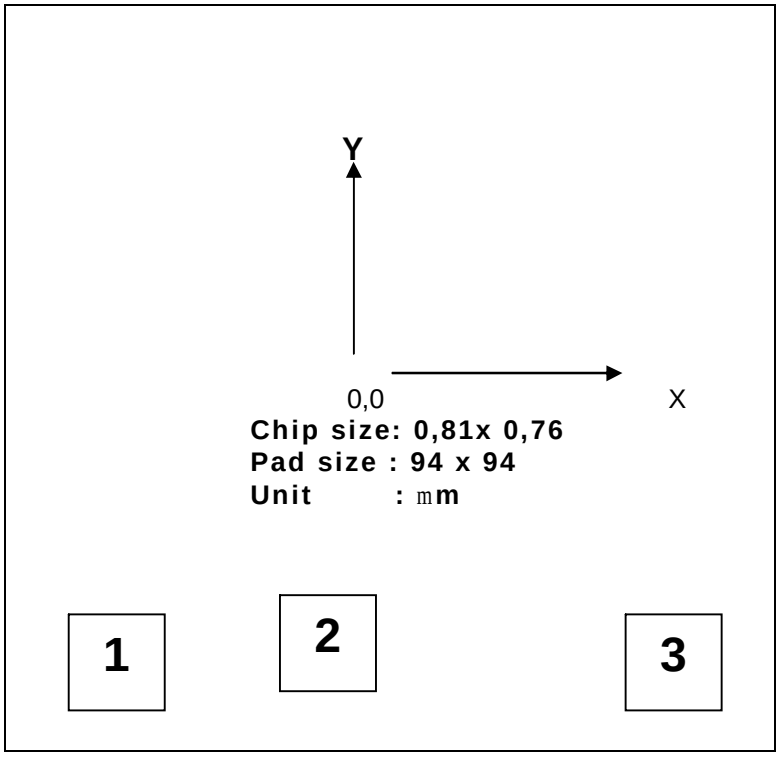


V_{KA} ³ V_{RE}

Fig.3. Test Circuit for I_{off}



PAD LAYOUT



PAD LOCATION

Unit: µm

Pad No.	Pad Name	Description	X	Y
1	R	Reference	-314	-299
2	A	Anode	-75	-275
3	K	Cathode	231	-299

PHYSICAL CHARACTERISTIC

Wafer dia	100 mm (4")
* Wafer thickness	280 … 420 ±20 µm
Scribe width	90 µm
Passivation	PSG
Backside metallization	Without metallization
Min. lot yield	75%
Min. wafer yield	60%

* The wafer thickness small be specified in a PO or Contract